REMARKS

This response and accompanying Petition for Extension of Time are responsive to the Office Action mailed October 3, 2003 (the "Office Action"). In the Office Action, claims 1-16 were rejected and claims 17-25 were withdrawn from consideration. By this amendment and without introducing new matter, Applicants have canceled claims 1-16, and have added new claims 26-60. For the purpose of advancing the application to allowance, Applicants have added claims 26-60 simply to provide clarification, to render explicit what was implicit, and to correct grammatical and spelling errors in the originally filed claims.

While the rejections under 35 U.S.C. 102(e) and 103(a) for claims 1-16 are rendered moot, Applicants dispute and traverse each of the rejections, and therefore provide the following response in an attempt to forestall any further rejections of the claims.

## I. Claim Rejections under 35 U.S.C. § 102(e)

Claims 1-5, 7-8, 10-14 and 16 were rejected under 35 U.S.C. § 102(e) as being allegedly anticipated by United States Patent No. 6,454,159 to Takushima (hereinafter "Takushima").

It is alleged that Takushima discloses forming a solder bump by dipping an electrically conducting core into a bath of molten solder. Applicants assert that this characterization is in error. Takushima discloses a "plurality of recesses ... formed in a solder transfer plate." The recesses described are similar in size to the electrodes being applied with solder (i.e. they are minuscule). A typical solder bath is much larger, and is generally designed to apply solder to an entire component or a large portion thereof. Applicants assert that no one of ordinary skill in the art would understand the recesses of those solder plates to be a solder bath.

Furthermore, Takushima discloses the application of solder to the solder transfer plate using a "powder or paste form" (col. 4 lines 24-25) perhaps using a "paste printer" (col. 4 line 30). Applicants doubt whether solder could be applied to such a solder transfer plate by dipping in a solder bath, as gases trapped in the recesses could prevent entrance of solder therein. And even if possible, such application differs significantly from the originally filed and pending claims.

Additionally, Takushima requires a precise alignment between the transfer plate and the contacts for which solder is to be applied (see col. 4 lines 37-40 and 63-67). A misalignment of the transfer plate would cause either damage to the contacts or a mis-application of solder thereon. The original and pending claims do not require alignment at this level (i.e. at a similar precision as the dimensions of the contacts) as solder may be applied to the entire contact surface with little required precision.

Applicants further submit that all of the methods disclosed by Takushima include the use of a mask in the course of applying solder to the semiconductor component, as the methods disclose using powder or paste using a paste printer. Solder is not applied to the surface of the entire transfer plate, but only into the recesses (col. 4 lines 21-22 "filled in the recesses 18 formed in transfer plate 16, as seen in Fig. 1"; fig. 1 shows solder only in the recesses). The solder composition must therefore be masked to avoid depositing solder to places other than the recesses. The transfer plate embodies a mask, which includes the portions of the solder transfer plate not being recessed (where solder is not deposited). In contrast, the pending and original claims lack any such mask component.

## II. Claim Rejections under 35 U.S.C. § 103(a)

Claims 6 and 9 were rejected under 35 U.S.C. § 103(a) as being allegedly unpatentable over Takushima as applied to claims 1-5 and 6-8, and further in view of United States Patent No. 6,440,835 to Lin (hereinafter "Lin"). Lin allegedly discloses coining a metal stud after it has been formed on a component. Applicants assert that Lin does not disclose the coining of a stud, but rather the coining of a "ball bond connection joint" through which "the tail can be reduced or eliminated" (col. 14 line 18). Applicants argue that the function of this coining operation is to reduce the profile of the tail rather than to enhance the adherence of solder to a stud. Applicants therefore maintain that a motivation to combine Lin with Takushima is absent, and furthermore the combination of Lin with Takushima would not yield all the limitations of claims 6 and 9.

Claim 15 was rejected under 35 U.S.C. 103(a) as being allegedly unpatentable over Takushima as applied to claims 1-5, 7-8 and 10-14 above, and further in view of United States Patent No. 6,395,983 to Gutierrez (hereinafter "Gutierrez"), with allegations that Gutierrez discloses soldering leads by wave soldering. To the contrary, Gutierrez does not disclose forming solder bumps on studs by wave soldering, but rather dip soldering and wave soldering "joined leads" (col. 7 lines 13-19) of toroidal induction coils (col. 4 lines 61-67) in a DIP package. It should be appreciated that a DIP package is characterized by pins that are set at a 0.100 inch pitch, and the "joined leads" as spoken of in Gutierrez are on a similar scale. The joined leads are first twisted and then soldered to make an electrical connection in-between. Applicants assert that one of ordinary skill would not look to a reference teaching of soldering "joined leads" of toroidal induction coils to discover how to form solder bumps on electronic chip contact pads. Thus, there is no motivation to combine Gutierrez with Takushima.

In addition to the arguments presented above supporting the assertion that the claims as originally filed would have been allowable over the Takushima, Lin, and Gutierrez, Applicants maintain that new claims 26-60 are allowable over those references for at least the following reasons:

For new claims 26-60: None of the cited references disclose (1) exposed contact pads with a non-wetting surface between and (2) bringing the entire interconnection surface in contact with molten solder.

For claims 29, 44 and 56: None of the references disclose forming a protruding electrically conducting core formed by a gold wire of about 25.4 μm diameter.

For claims 30, 45 and 55-60: None of the references disclose the coining of a metal stud (Lin discloses the coining of the tail of a ball bond connection joint rather than a stud.)

For claims 31, 46 and 57: None of the references disclose the stacking of a plurality of studs by wire bonding.

For claims 32, 47 and 55-60: None of the references disclose the formation of solder bumps on a core having a dimension of 75 μm or less without any bridging in between.

For claims 33 and 48: None of the references disclose the dipping of the entire interconnection surface into a bath of molten solder.

For claims 34 and 49: None of the references discloses the application of molten solder to the entire interconnection surface through a wave soldering process.

For claims 35, 50 and 55-60: None of the references disclose contact pads having cores and solder bumps spaced at a pitch of about 150 μm or less.

For claims 36, 42-54 and 55-60: None of the references disclose applying solder to the entire interconnection surface to form solder bumps on studs on a plurality of electronic chips on the same wafer.

For claims 37, 42-54 and 55-60: None of the references disclose dicing the wafer into individual chips after the application of solder to the entire interconnection surface to form solder bumps on studs on a plurality of electronic chips on the same wafer.

For claims 38, 51 and 58: None of the references disclose the step of repeating the contact of the interconnection surface with molten solder to increase the size of the solder bumps.

For claims 39 and 52: None of the references disclose the assembly of an electronic connection between two components with the configuration of solder bumps formed on studs.

## CONCLUSION

Applicants respectfully assert that claims 26-60 are allowable. A petition for a two-month extension of time in the amount of two months, extending the period for response to March 3, 2004, is enclosed with this response. Please grant any additional extension of time required to enter this response and charge any additional required fees (beyond the enclosed check) to Deposit Account No. 50-0581.

Respectfully submitted this 3rd day of March 2004.

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